AMRAD NEWSLETTER

Amateur Radio Research and Development Corporation

June 1982

ON MONDAY, JUNE 7, IN VIENNA, VA the 1982 Science Fair Award Winners will be presenting short talks on their projects. We judged at the two Fairfax County Fairs and the Regional Fair at Wakefield H.S. this year. I would like to thank the following members for devoting Saturday mornings to this effort: Eric Nyman, Howard Batie, Elton and Nancy Sanders.

The Award Winners and their project titles are as follows:

Thomas Falstreau	Computer Aided Instruction
Steven B. Waltman	A Computer Controlled Nuclear Magnetic Resonance Spectrometer
J. B. Wilson	Paddle Battle-A Computer Game

Each of the winners will receive a subscription to the computer or radio magazine of their choice in addition to student membership in AMRAD. This promisses to be an interesting evening with plenty of good color graphics.

The meeting will be from 7:30 to 9:00 P.M. in the Patrick Henry Branch Library, 101 Maple Ave East, (VA Rte 123), Vienna, Virginia. Visitors and guests are welcome. - Bill Pala, WB4NFB

WE REGRET THE ERROR in the May newsletter which showed the meeting date at May 5. It should have read "May 3." Unfortunately, some members came on the 5th.

OUR NEXT MEETING DATE WILL BE MONDAY, JULY 19, not July 5. The reason is that the Fairfax Library Hq has not yet decided whether July 5 will be a holiday for the libraries. So, mark July 19 on your calendar, as well as the following dates for the rest of 1982:

August 2
September 20 (The 6th is Labor Day)
October 4
November 1
December 6 - AMRAD Annual Meeting -

THE MANASSAS HAMFEST will be on Sunday, June 6 at the Prince William County Fairground, 0.5 mi south of Manassas, Virginia on Rte 234. Gates are open at 7 A.M. for tailgaters ($3 per space) and at 8 A.M. for general admission ($4). The talk-in frequencies are 146.37/146.97 and 146.52 MHz.

THERE IS NO PROTOCOL COLUMN BY DAVE BORDEN in this issue because Dave is California at press time. However, look for an article by Den Connors, KD2S on the new Tucson Amateur Packet Radio protocol in this issue.

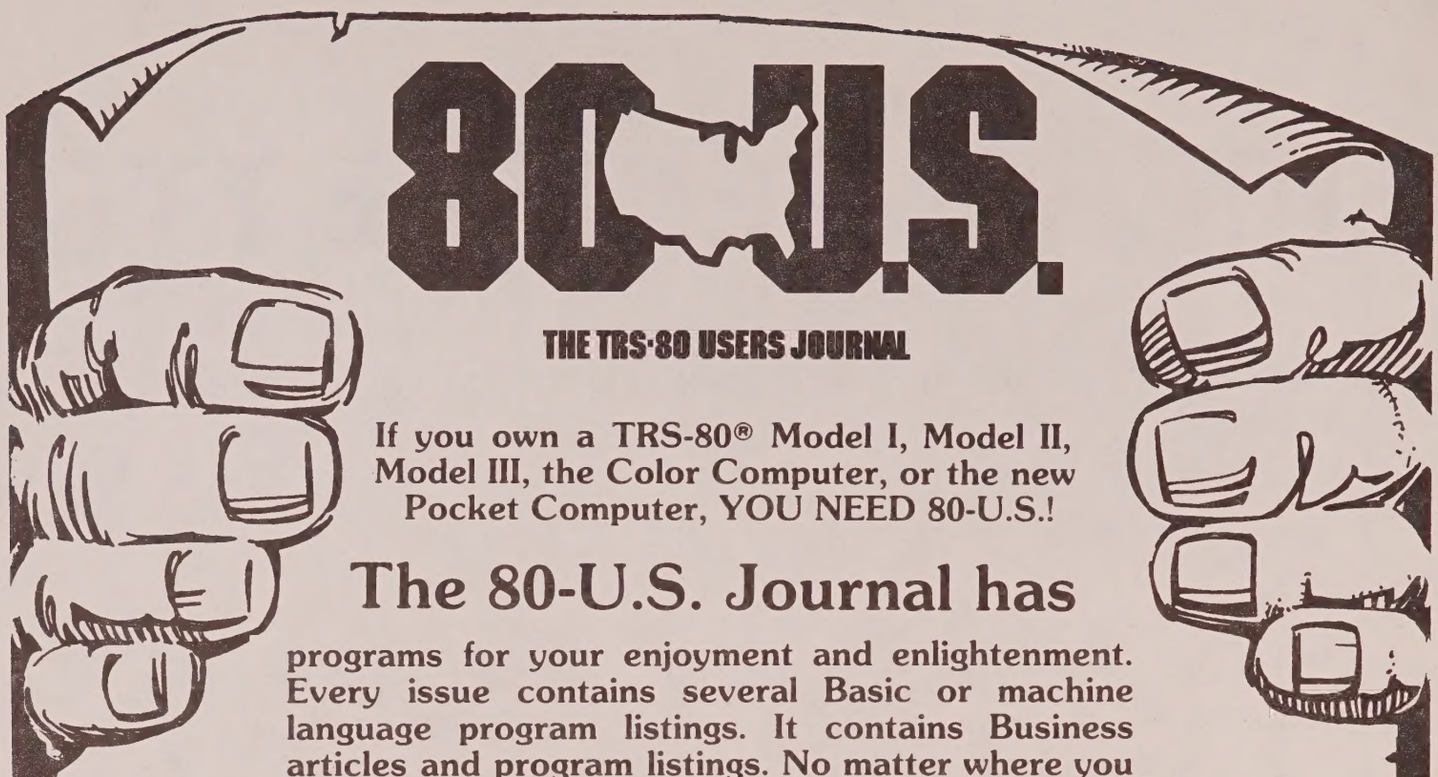
WHILE SOME OF US WERE ENJOYING DAYTON, Terry Fox, WB4JFI had to stay close to home and used that time to develop a memory-expansion modification for the VADCG TNC board. See Terry's article in this issue. In addition, he has developed a method of software control of the VADCG TNC board baud rate without disturbing the cw i-d speed. Look for an article on that next month.

THE LIMARC/IEEE TECHNICAL TALK on May 12, on Local Area Networks, heard on AMRAD's WD4IWG/R, was the last one of this season. On May 12, the network included Long Island, New Jersey, Michigan, Boston and Washington, DC. In case you missed it, the speaker talked for about 10 minutes then paused for questions/comments from the listeners. Plans are to reactivate the talks in the fall. People willing to provide program material for future sessions should contact Ed Piller, W2KPQ at 516-349-2484 (work), 516-938-5661 (home). Thanks to WB4WLW and W4VA for arranging the link-up at this end.

TWENTY 8273 PROTOCOL CHIPS were provided to AMRAD at no cost to us for distribution to experimenters within certain restrictions. All are early date codes which are believed to be good and have been checked out in packet repeater service on a VADCG TNC board for satisfactory operation (however, no guaranties!). They are to be free (except for mailing costs), only one per person, for use by that person, and not for sale to someone else. We further ask that members request one only for packet controller boards that they plan to build in the immediate future, not for indefinite future use or for a spare. Please request by letter stipulating that the 8273 will be used by you personally and will not be sold, and include a check in the amount of US$1, payable to AMRAD, to cover mailing costs.

YOU CAN NOW CONTACT AMRAD VIA ELECTRONIC MAIL on MICRONET [72345,1050], which is serviced by Bill Pala, WB4NFB.

A SINGLE-CHIP FSK MODEM has just been announced by Advanced Micro Devices Inc. Called the Am7910, it has built-in A/D and D/A converters and a digital signal processor with 24k of ROM and 1.3k of RAM for filtering. By selecting among 5 mode-control lines, the chip can become a Bell 103 originate, Bell 103 answer, Bell 202 with/without equalizer, CCITT V.21 orignate or answer, or one of several modes of V.23. According to Mike Stauffer at AMD, samples will be available in mid-June with production units to follow in August or September. Single-unit prices are expected to be in the $35-40 ballpark initially. For more information, contact AMD or see Mike Stauffer's article in the May 12 issue of EDN magazine.



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Tucson Amateur Packet Radio Activities

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As summer continues down here (it starts months before other people's summer), we finally are playing with our own boards! We are very busy with the software effort, and have been modifying hardware design, layout, protocols, etc. as the Alpha test nears completion. See Lyle's hardware report for some of the details.

TAPR will be looking for groups of hams who are interested in helping us with testing the Beta version of our board, to prove the system in real environments, and find improvements in the protocol required to handle real-life problems. We also are setting up a second set of tests, to be performed by the same or additional Beta test sites, using software provided by some standards agencies to determine the applicability of different standard protocols in a packet radio environment. We believe this kind of experimentation is very important for amateur packet radio at this time, and performs a unique service, providing a testbed far larger than these agencies could ever hope to realize.

Our programming effort has shifted now to developing the FORTH primatives for interfacing to the on-board components, and to creating the state sequences necessary to effect the dynamic addressing protocol we have chosen for our first efforts. The higher-level routines are written, and the VADCG-compatibility program elements will also be worked on this month.

TAPR Hardware Report

Alpha boards are here! The PC released the boards on April 5th, and during the next several days the twelve Alpha testers took delivery of boards, documentation and brown paper sacks filled with parts. Soon the sacks were empty and the boards full. Those of you who were at Dayton got a sneak preview of an Alpha board, courtesy of Pete Eaton, WB9FLW. And we certainly appreciate the constructive comments made at Dayton regarding the TAPR TNC --wait 'til you see the Beta boards!

Due to some job commitments, forced travel, examinations and other events that somehow get in the way of more important things such as Amateur Radio, the Alpha test phase is a bit behind schedule, to no one's complete suprise. Nonetheless, considerable progress has been made. By May 8, the following Alpha-level hardware goals had been achieved:

* interface of the TNC to a variety of terminals/computers
* self-test at power-on with status report
* activation of the HDLC controller
* activation of the cw i-d facility
* verification of parallel port operation
* verification of NOVRAM interface
* verification of the watchdog timer function
* verification of the modem design and interface
* on-board calibration of modem frequencies to ±5 Hz.

In addition, a major software achievement was realized on May 1, when N7AIG, aided and harassed by WA7GXD and Mark Baker (TAPR secretary, no call yet), got an advanced version of STC FORTH running on the TNC in a standalone configuration. This was a major test of N7AIG's MetaFORTH target compiler (running on his Apple), and Dave's efforts have made the Hardware Committee's debugging and low-level driver coding tasks much easier.

It is now anticipated that TNC's will be talking to each other in the very near future. Hardware efforts will then turn to Beta activities, including a meeting with the Computer-Aided Design (CAD) boys for possible computer-generation of the Beta artwork. Component suppliers are beating our doors down in an attempt to make the Beta (and beyond) boards lower in cost, and We're listening! Our goal is to make the TNC, as well as future developments, available to the entire Amateur Community on a non-profit basis. (Yes, we are capitalists, but we just don't beleive in making money off of our Amateur bretheren.)

Now for a look at the microprocessor side of the TNC design.

The TNC has a specific mission -- implement the lowest layers of packet protocol. Since the definition of these layers is in a state of flux, the TNC must be very adaptable. This implies programmability, and in today's world, this means a microcomputer. Thus, the TNC is a small, dedicated-function computer.

Naturally, virtually every silicon foundry has a pet microprocessor (uP) and they are not necessarily compatible with each other. Every family in the microprocessor world has its unique, special function peripheral parts, and some of these are very useful in the specific case of a TNC design. The rub comes when a project requires the use of a certain uP, and the uP chosen by (or forced upon!) the designer lacks the right peripherals. Then there are manufacturers who just make sophisticated peripherals that won't directly interface with anyone's uP -- such parts are called "universal".

It happens that, within TAPR, the majority of the group have a soft spot for the Motorola architecture, and some clever people at Commodore made up a uP that is bus-compatible (that means that the hardware interfaces the same) with the Motorola family (6800, 6802, 6809) and the uP they made, called a 6502, is very popular. Every Apple, PET, Atari, AIM, KIM and SYM has one. So does the TAPR TNC.

The 6502 family incorporates some powerful peripheral chips, such as the 6551 UART (with baud-rate generator) and the 6522 Parallel Interface (with dual 16-bit timer/counters), both of which are on the TAPR TNC. The family does not include a good HDLC controller (good means on-board PLL for clock recovery from NRZI data as used by nearly every packet group).

Meanwhile, on the other side of the uP architecture, Intel and others have their own families, and were responsible for pushing through a memory standard endorsed by JEDEC (which doesn't necessarily mean much), and many manufacturers have jumped on this bandwagon. The concept is called "bytewide", and it makes for a universal socket that can take ROM, EPROM, EEPROM and RAM. It uses

THE DEAF AND THE TTY

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TDDs in Europe

This month I had the occasion to be in the company of a prominent deaf leader from Switzerland. Accompanying him was an engineer knowledgeable in telecommunication matters.

It was very interesting to learn of what he had to say about telecommunications in Europe. And I am sharing this with you, because perhaps some of you had contacts with Europeans with radio-related matters.

First, there are TTYs, only TDDs in Europe. TTYs refer to mechanical teletypewriters (reconditioned machines of the Model 15, 28 variety), while TDDs refer to portable devices. One major reason for this development is that either the post offices or the governments control these TTYs, and are not partial towards surplusing these to the deaf people.

The prices of the European TDDs are exorbitant, costing from $1,000 to $1,500 per device, as compared to $500 to $800 in the States. It is not because our dollar is cheap out there, but because of fierce nationalistic pride. TDDs made in Italy are rejected in France; or German TDDs are sneered at by Swedes, and vice-versa. These natives prefer to buy products made in their country if at all possible. Limited country-by-country production boosts prices high.

Compatibility is another matter. While the code that they use is ASCII (Baudot, a French name is nonexistent), the baud speed is different. Most of Europe is on 110 baud, but Sweden is an exception as it uses 300 baud.

In England, the Post Office, when they were operating the communications system, adapted the Prestel teletex system in telephone communications. The existing British TDDs, called Kegwain DCT, are incompatible with Prestel devices. The keyboards differ by only one letter. The Z is where the Y is in our sets.

There are about 80,000 TDDs in the States, but it is alarmingly low when compared to the numbers of profoundly deaf people. If we take half a milion profoundly deaf as an approximate population count, then the ratio is 16 TDDs per 100 deaf people. In Europe, since the adult deaf population of a typical country runs into low thousands (for example, only 3,000 deaf adults in Sweden), then the TDDs per 100 deaf people radio is lower, though statistics are not available.

Because the standards differ between Europe and the States, and even among the European nations, communicating is to mis-communicate.

TAPR (continued from previous page)
a "two-line" control, which is nice for them and bad for the Motorola types. (Heh, heh -- very clever.)

Another outfit, called Western Digital, makes smart peripherals for doing things like HDLC control. Rather than take sides, they use an Intel-like control structure, but invert all the lines so the HDLC chip will need TTL "glue" with everybody's uP. Then they undercut the market with pricing so designers can buy some TTL and still save money!

With this background, the TAPR Hardware group appeased the majority by using the 6502 (in all fairness, a good chip, and one that has a lot of software development behind it within the TAPR infrastructure), the bytewide memory standard and the Western Digital HDLC controller. (For those who may be concerned about the compatibility of the WD 1933 chip with the 8273 used on the Vancouver TNC, let me point out that the KA6M repeater in San Fransisco uses the 1933 chip.) As it turns out, the TTL glue needed to tie all of this together, including the clock generator, comes out to four packages, plus a Shottky PROM used for address decoding to allow any mix of RAM/ROM sizes in the bytewide memory area. Alpha TNCs are set for 2 2k-by-8 RAM's and 4 4k-by-8 EPROMS, but the sockets can handle up to 8k-by-8 parts, and the address decoder can be changed very, very easily.

The net result is a TNC that is easily reprogrammable (in a high-level language called FORTH - but that is another issue), capable of using the latest technology in memory components for future expansion and very economically priced due to the use of multiple-sourced parts.

Next month we'll try to highlight some of the hardware-oriented goals of Beta test, as well as report on Alpha progress.

Meanwhile, if you happen to be in Southern California during the weekend of June 4-6, be sure and come to the ARRL Southwestern Division Convention and San Diego Computer Fair — TAPR will be there in force, with operating TNC's. Saturday morning will include a full session on packet radio, with participants from all over. We're looking forward to a great time, and hope to convert many an ASCII/RTTY buff to packet. Hope to see YOU there! 73 from the TAPR Hardware gang
Lyle Johnson, WA7GXD

TAPR Protocol Report

Last month's AMRAD newsletter included comments and comparisons of Terry Fox's protocol proposal and the TAPR protocol. The TAPR effort has been modified heavily since the last (December) release, and now complies very nicely with "standard" protocol and interface definitions. Take a look at my article in this newsletter on protocol for more information on what TAPR will be doing.

And So On

Mike Parker and the Microwave Committee have performed initial tests on the type of transverters that AMSAT plans to use to access the L-band transponder input on phase IIIB, using an AMSAT-supplied box sent down here a couple of weeks ago. Preliminary design should be completed before the next newsletter. Volunteers for Beta testing are still being sought.. we currently have fifteen major cities lined up, with more due, but the first Beta distribution will be pretty much settled before next month.

Stay tuned for more reports on local and national activities of the TAPR group!
73, Den KD2S

Protocol Exposed

(or "Why I don't Talk to Myself")

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I don't normally talk to myself, but if I do I never listen anyway. At least normally. But after several weeks of very heavy labor both at work and for TAPR, I found myself discussing things in my brain.

"Self," I said,"I'm really proud of how well the different groups involved in packet radio have done to date. Did you notice that We're all using standard protocols?"

"Excuse me, but I'd like to see how I came to decision!"

"What do you, I mean me, mean by that? The VADCG group has chosen HDLC, and AMRAD is working on an ADCCP package. Even TAPR is looking at a subset of the IEEE-802 LLC (logical link control)."

"Look again... How often do you guys read those standards? The first two bit-oriented protocols were never designed for local area network use. They were meant for a primary point to link to one or more secondary points, on a dedicated line. Which groups send a continuous stream of frame flags or "breaks" down the line when the primary's not transmitting?"

"Well that's just a stupid thing to do on a radio channel. Of course none of us block the channel!"

"Yet you'll find that in the HDLC standard. Never mind. Answer this then: All of the protocols involved presume the address of the primary, and so ALL addresses are that of the secondary, receiving station. I don't recall that the above-mentioned groups are placing the receiving station i-d in their packet address space at all."

"Well, that's true. The i-d used is always that of the sending station instead."

"That's right. So none of you hams are using some fundamental aspects of these protocols. It's a good thing too."

"Why do you say that?"

"You guys are misusing these protocols to let you get onto the radio channel with packets. You change the standard around to reflect the fact that there's a repeater on channel who will be instrumental in routing the packets, based on initialization schemes using the control field. The medium is not one of a primary in control of slaved secondary stations. It's one of multiple primaries, or nodes, all with the power to initiate conversations at will."

"OK, so we don't run HDLC, or ADCCP or whatever. But notice that I said TAPR is using a subset of LLC, a brand new protocol DESIGNED for local area networking! I think we have the jump on all the other groups!"

"Think again Charlie. What you guys will be using is a dynamically assigned, single-byte addressing scheme with both the sender and receiver i-d in the packet header. That allows a balanced mode of operation, but ADCCP and a few other protocols allow balanced modes without double addressing anyway. Your problem is that the IEEE standard also calls for a "medium access layer" sitting smack dab between the physical and link layers, and that layer is more complicated than anything any of the ham groups have come up with yet! I think you'll find that using a protocol designed for a 10Mb/s link would be just as bad as using one for point-to-point. All groups are justified in using whatever "sub-set" of whatever protocol they want, since there is no standard designed for slow packet radio channels!"

"Sigh.. I guess we're not at the point yet of defining a universal standard for balanced-mode transmissions on a shared medium that doesn't lend itself to simultaneous collision detection, true?"

"I'm glad you said that... Sounds like you hams have a lot of work ahead of you in figuring out what will work best. Keep up with protocols BASED-ON, but not compatible with, the standards already out, and the controller chips will help you out financially. The IEEE will have some standards for broadband coaxial cable networks in the near future, and the head-end translator looks a lot like a repeater.... Keep up the experimentation..."

"OK. Now can I go to sleep?"

TAPR PROTOCOL

The Tucson Amateur Packet Radio group will be using a protocol based on standard segmentation of networking tasks into levels of protocols with well-defined interfaces between levels.

Phisical Level

The physical medium includes medium access procedures, specifically using carrier-sensed multiple access on a channel which may have, but does not require, a simplex digital repeater. The two tones used by the Bell 202 standards will be used for mark and space, and NRZI encoding will provide for synchronization of the incoming packet to the demodulator.

Link Level

The data link layer operates on the physical channel, controlling access and utilization. Specifically, the link layer handles:

- control of data transfer
- error checking and recovery
- information coding
- information transparency
- optimization of channel utilization
- maintenance of synchronization
- communication facility transparency
- remote node bootstrapping capability

A "sub-set" of the IEEE-802 Local Area Network Standard is used, a combination of the Logical Link Control and Medium Access Control. Medium Access (MAC) fits within the LLC packet, and may be used to handle a large number of medium specific problems which simply cannot be handled by the point-to-point and multi-drop bit-oriented protocols currently in use. Multiple control stations, nodes located in multiple local area network domains and other problems of this ilk can be controlled by expanding header bytes beyond the control byte. →

The control patterns used in the control byte are defined by LLC, and are identical to those of HDLC, SDLC, ADCCP and others. There are two address bytes, those of the sender and receiver, allowing non-repeater and repeater operation. The addresses are given to nodes at the time the node enters the net by the first station on the channel. This station, designated the Net Control or Station Node, is identical to all other nodes on frequency, except that it parcels out addresses for nodes checking in, and distributes to all nodes current addressing information. By default then, any stations leaving a net immediately lose their i-d, and are given a new i-d upon arriving at any new network. If no net exists on frequency, that node becomes the net control. No multiple address problems are possible in this type of addressing scheme; if a system failure occurs, however, the net control simply reassigns i-d's to violating nodes. Note also that all information for giving out i-d's is available at all nodes, so that the loss of the net control is handled trivially by the first station detecting loss picking up the NCS .

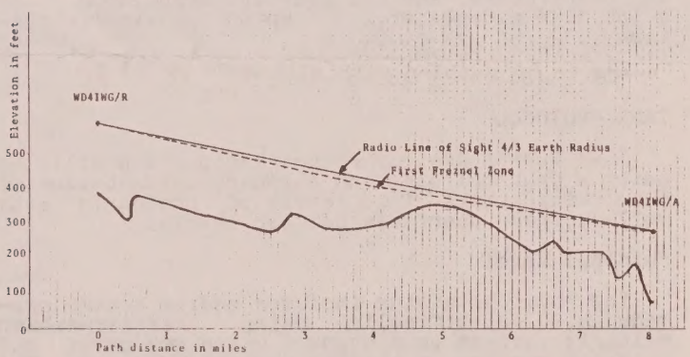
Network Level

The current network layer must handle the functions normally associated with control of the local area channel, transport of messages and interfacing applications programs for these early networking experiments. Specific functions handled by this layer are:

support of datagrams and virtual circuits
opening and closing connections
data transfer
error control
message flow
routing of messages to destinations

The mechanism for flow control is the simple stop-and-go type of algorithm, identical to other packet implementations. Certain of the functions called out are also found in the link-level protocol, since these hooks are required to pass the functions through the channel. There will be more on this protocol written in the TAPR activities column by the Software Group, as "things develop".

A REMOTE RECEIVER IS TO BE INSTALLED IN ROSSLYN in the next few months to provide better coverage of downtown Washington, DC and the Potomac River area. This should permit users with handheld transceivers to get into the AMRAD WD4IWG repeater from locations such as The Mall, The Capitol, National Airport and The Pentagon. We wish to acknowledge the support given us by Xerox Corporation for the receiver site in Rosslyn and to Joseph E. Posch, WA4FXN who made the arrangements. T-MARC coordination was obtained for a 440-MHz auxiliary link frequency to connect WD4IWG/A (Rosslyn) to WD4IWG/R (McLean). WB5MMB and W4RI were able to communicate from the WD4IWG/A site through WD4IWG/R with IC-2AT HTs on low power. Below is a profile of the path between the two sites:



TWO ULTRONIC DATA PUMP 202/1200 Bell 202-compatible modems, with built-in power supplies, are available from Paul Rinaldo, W4RI, for $50 each. They have not been tested but look ok and are offered on an as-is basis. Documentation is available. For pick up only in McLean, VA (not shipment), call 356-8918.

A SILCLAIR ZX80/ZX81 USERS GROUP has formed in Northern Price Georges County, Maryland. They plan to meet on the second Saturday of each month in members' homes. Please contact Don J. Reed, WB3FUE, 4330 Hartwick Rd #616, College Park, MD 20740.

COMMODORE VIC-20 COMPUTER USERS interested in VIC-to-VIC QSOs and trading VIC-20 software may wish to contact Dennis E. McCormack, K1PLX, P.O. Box 981, Salem, NH 03079. Also, Fred N. Howard, W6ORF, 1338 Valley View Rd, Glendale, CA 91202 would like to contact someone who can give him information on how to interface his VIC-20 with his RTTY set-up.

ANYONE NEAR LANCASTER, PA FOR 1200 BAUD? W3FEY writes that he has a Cermetek modem about ready to go. He adds that N3AY, K3NCY and WB3CSY are all working on 1200-baud modems. He would like to know if anyone has an Altair 8800B for sale. Contact George Gadbois, W3FEY, 141 Maple Ln, Lancaster, PA, 17601, 717-397-0158.

AN AMICON TELECONFERENCE was held on March 27 for the purpose of advancing the planning of the AMSAT International Computer Network. Representatives of AMSAT, AMRAD, Tucson Area Packet Radio, Bay Area and Northern New Jersey Packet Radio Groups participated.

The special conference bridge was prepared by W4OWA and donated by AT&T for AMSAT use in furthering Amateur Radio satellite objectives. It was the same type of bridge which afforded the amateur radio world the excellent coverage of UoSAT-OSCAR 9's launch last autumn.

Hank Magnuski, KA6M, who is AMICON System Engineer, represented the Bay Area. Den Connors, KD2S, spoke on behalf of the Tucson group. Steve Robinson, W2FPY, who is AMSAT's Director of Research and Development, spoke for the Northern New Jersey group. Paul Rinaldo, W4RI, President of AMRAD, represented that organization. Representing the Operations Directorate of AMSAT were Rich Zwirko, K1HTV, Operations Vice President, and Bob Ruedisueli, W4OWA. Vern Riportella, WA2LQQ, AMSAT Executive Vice President, chaired the meeting.

The meeting focused on key issues concerning start-up of AMICON operations of the Phase IIIB SSC (Special Service Channel), what types of modulation should be used for an interim standard; for a long-term goal; protocol updates and compatibility questions; local area net interfaces; potential for inter-SSC collision. The meeting lasted for about 90 minutes. Specific follow-up actions were to be taken by KA6M, W4OWA, KD2S and K1HTV. Future meetings of this type are to be held. Everyone present indicated they were gratified at the progress made. Thanks, AMSAT Satellite Report.

THE VIRGINIA TELETYPE SOCIETY was mentioned in A5 (Amateur Television Magazine). The item stated that the WB4JBJ repeater on 147.705/105 MHz has a link to W4PNT/R which operates on 147.675/075 MHz. Operation is normally Baudot (2125/2295 Hz tones), but ASCII is operated on Thursdays and Sundays. We wrote to Larry Lewis, WB4JBJ to open discussions on possibilties of setting up 220-MHz packet radio repeaters from Northern Virginia down to North Carolina. Larry subsequently visited Northern Virginia and checked in on the AMRAD 147.81/21 repeater. He said that there was no packet radio activity in his area but that one or more of the RTTY amateurs would be interested in learning more about it. We hope to follow up with VTS and realize that it will take quite some time to line up all the needed resources.

MORTTY, an "advanced communications program for the H8, H89 or Z89 with HDOS," has been announced by Phillip L. Emerson, 3707 Blanch, Cleveland Heights, OH 44118. The program includes ASCII and Baudot and runs at as many baud rates of which the equipment is capable. The price is $100.00.

VADCG TNC Modifications

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I have found that we are rapidly approaching the limits of memory on the Vancouver Amateur Digital Communications Group (VADCG) Terminal Node Controller (TNC) board. It is just barely able to handle the link level software in the four 2708 EPROMs used on the board. This means that any network-level software must be done external to the TNC board. One approach is to come up with a new TNC board that has more memory on it, both RAM and EPROM. The other option is to expand the capabilities of the VADCG TNC board. I should point out at the outset that this modification is a kludge, but at least it works! Only one IC is added to the board, and it is put on the board dead-bug fashion (upside-down).

This modification is done in two parts, first the RAM on the board is moved from its present location (1000-1FFF hex) to a new location to allow more EPROM memory. The new location is 8000-8FFF hex, which should allow up to 32k of EPROM memory. This location also simplifies the hardware modifications required. The second half of the modification changes the EPROM sockets to allow the use of either 2716s or 2732s.

Relocating RAM to 8000 Hex

This part of the modification requires the addition of another IC, called U27, which can be either a 74LS138, or an 8205. U27 becomes the RAM address decoder, while leaving U8 the EPROM address decoder. I should point out that the schematic that I received with my VADCG TNC board has some minor errors. One of these is that address lines A8 thru A15 from the 8085 (IC-1) are backwards. A15 is pin 28 of the 8085, A14 is pin 27, etc... down to A8 being pin 21. Using the proper pins is important to this modification, so be careful of this error.

When this portion of the mod is completed, the TNC should still operate using 2708s for the EPROMs. I recommend that the board be completely assembled and tested before doing any modifications. Have someone burn a couple 2708s with repeater software for your call in them, one version for RAM at 1000 hex, and the other version for RAM at 8000 hex. Even if you don't use your board as a digital repeater, it is a good test of the TNC, and usually will fit in one 2708. Test your completed TNC to make sure it functions properly. Refer to Fig. 1, 2 and 4 while doing this mod. I have laid the mod out in steps to make it easier to follow and check off. Cuts on the board are shown as a small X thru a trace.

1. Cut traces between U8 pins 7,9,10,11 and U19 to U26 pin 8. The cuts are done by U8 with pins 7, 9, and 10 cut on the top (Fig. 1), while the pin 11 trace is cut on the bottom of the board (Fig. 2).

2. Cut the trace at U8, pin 5 to ground (Fig. 2). Hook U8, pin 5 to U1 (8085) pin 28 (A15).

3. Drill two holes as shown in Fig. 1. These holes facilitate the wiring of U27. Be careful not to drill thru any traces.

4. Add IC-27 (74LS138, or 8205) to the board as shown on Figure 1. It can be glued to the board if necessary, or use double-sided tape. Put a 16 pin solder-tail socket to it to allow replacement in case it should fail, and wire the pins as follows:

   A. U27 pin 1 (A0) to U1 pin 23 (A10).

   B. U27 pin 2 (A1) to U1 pin 24 (A11).

   C. U27 pin 3 (A2) to U1 pin 25 (A12).

   D. U27 pin 4 (E1) to U1 pin 34 (IO/M*).

   E. U27 pin 5 (E2) to U7 pin 11 (RD/WR)

   F. U27 pin 6 (E3) to U1 pin 28 (A15).

   G. U27 pin 8 (GND) to ground bus as shown.

   H. U27 pin 12 (O3) to U25+26 pin 8 (CS*) at cut

   I. U27 pin 13 (O2) to U23+24 pin 8 (CS*) at cut

   J. U27 pin 14 (O1) to U21+22 pin 8 (CS*) at cut

   K. U27 pin 15 (O0) to U19+20 pin 8 (CS*) at cut

   L. U27 pin 16 (+5V) to +5 volt bus as shown.

Now that U8 is only used for EPROM's while U27 is used for RAM, U8 doesn't need to be enabled selectivly with WR, but just with RD from U1. U27 needs to be enabled with either RD or WR from U1. These changes are done by rewiring U7, the 74LS00 as follows:

A. Cut the trace between pins 3 and 4 of U7 on the bottom of the board (Fig. 2.) This trace is thick; so check with a meter to be sure it is totally cut.

B. Cut the trace between pins 6 and 10 of U7, located on the bottom of the board (Fig. 2).

C. Cut the trace between pins 14 and 13 of U7, also on the bottom of the board. This is also a thick trace; so check the cut.

D. On the top side, cut the trace from U7 pin 5 to the small feedthru as shown in Fig. 1.

E. Wire U7 pin 2 to U7 pin 4.

F. Wire U7 pin 5 to U7 pin 9.

G. Wire U7 pin 6 to U7 pins 13 and 12.

H. Wire U7 pin 10 to U7 pin 14 (+5V).

I. U7 pin 11 should be hooked to U27 pin 5 from step E of adding U27 above.

Double check your wiring. It should now match the schematic in Fig. 4. If it does, install the EPROM that has software for RAM at 8000 hex, and try out your board. If everything is working, the TNC should operate as if unmodified. If not, recheck your wiring for mistakes.

Your board now has the RAM relocated to 8000 hex which will provide a lot of address space for the new EPROM added in the next step.

Changing the EPROM to 2716 or 2732

Since there are only four EPROM sockets, the TNC is severely limited in how much software can be run. I feel that if a separate processor is used to generate and receive packets, it should be able to run most all of the networking overhead, not just the link level. The four 2708 EPROMs are

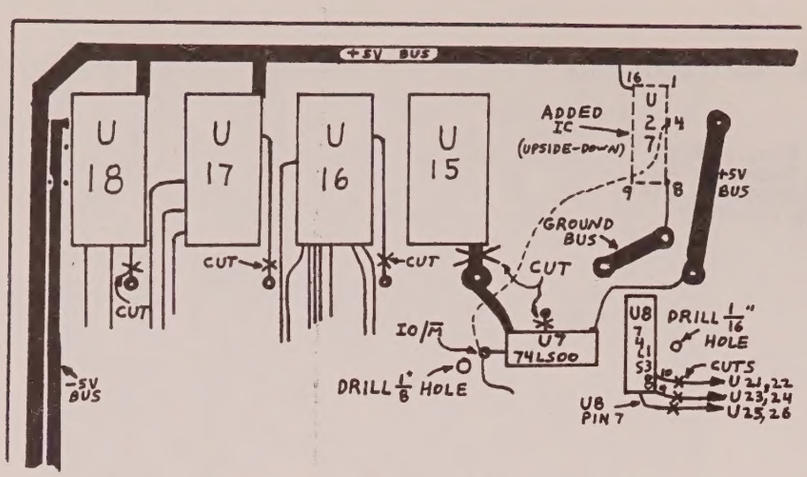

Fig. 1 - Top of board.

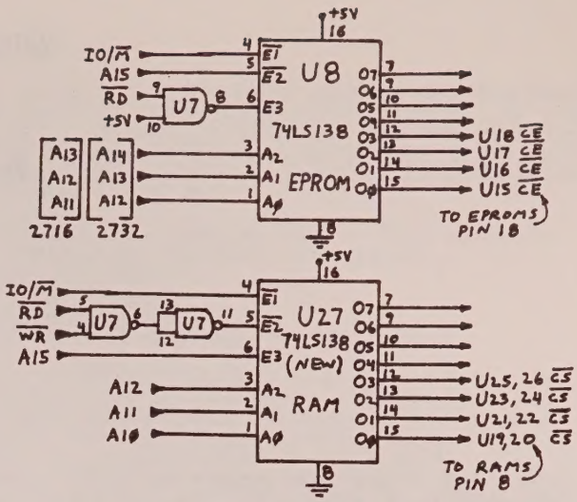

Fig. 4 - Modified memory decoder.

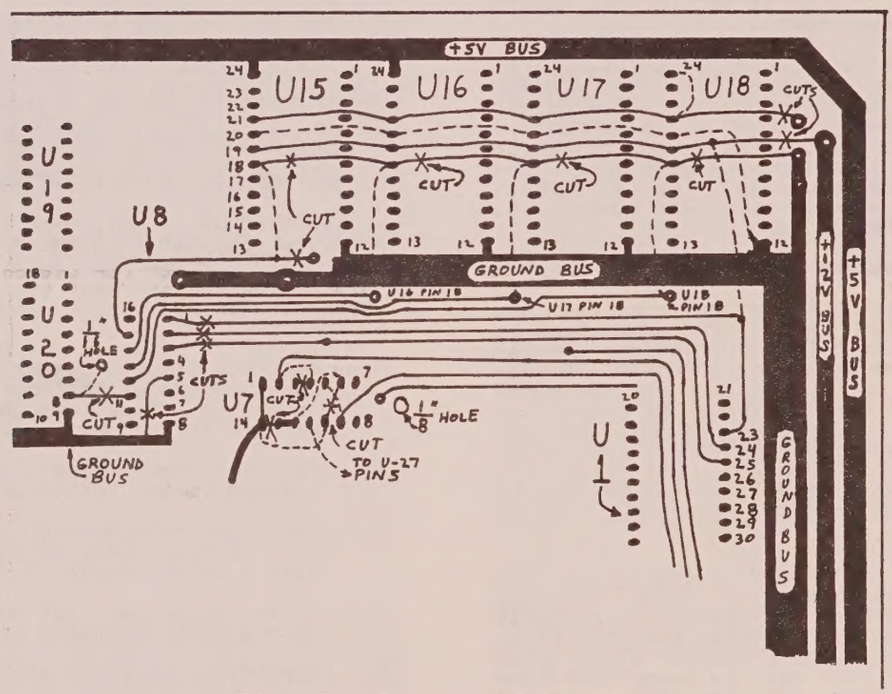

Fig. 2 - Bottom of board.

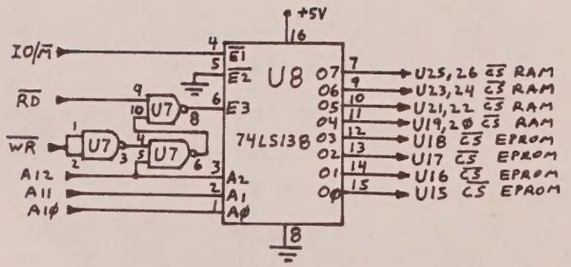

Fig. 3 - Original memory decoder.

PIN	27Ø8	2716	2732
18	GROUND	$\overline{CS}$	$\overline{CS}$
19	+12V	A10	A10
2Ø	$\overline{CS}$	GROUND	GROUND
21	-5V	+5V	A11

Table 1 - EPROM pin changes.

just about full with only a bare-bones version of the link-level software, so there is no room left for the actual network software or anything above that level. This mod will allow the use of 2716 or 2732 EPROMs instead of the 2708s being used. This will change the maximum EPROM capability from the present 4k to 8k (4-2716) or 16k (4-2732). An added feature of this mod is that the minus 5-volt power supply is no longer used, and can be eliminated.

Part 1 of this mod pertains to both 2716 and 2732 EPROMs, while part 2 should only be done for the type of EPROMs to be used.

Part 1, 2716 and 2732 Mods

Do this part of the modification for both 2716s and 2732s. Again, the mod is done so that your progress can be checked off.

1. Cut and isolate pin 18 of U15, U16, U17, and U18 from each other and from grounds at both U15 (top of board) and U18 (bottom of board).
2. Cut traces between U15 thru U18 pins 20 and U8 pins 15 to 12. Wire as follows:
   - A. U15 pin 18 to U8 pin 15.
   - B. U16 pin 18 to U8 pin 14.
   - C. U17 pin 18 to U8 pin 13.
   - D. U18 pin 18 to U8 pin 12.
3. Cut the trace hooking U15 thru U18 pin 19 to ground at some point between U18 and the ground bus. Hook the U15 to U18 pin 19 trace to U1 pin 23 (A10).
4. Wire U15 thru U18 pin 20 together and tie them to ground.
5. Cut the trace hooking U15 thru U18 pin 21 from the -5 volt bus between U18 and the -5 volt bus as shown.
6. Cut the traces at U8 pins 1,2, and 3.

Part 2, 2716 Wiring

5A. Hook the trace of U15 thru U18 pin 21 to a +5 volt bus (U18 pin 24 is OK).

6A. Wire U8 pin 1 to U1 pin 24 (A11). This can be done by hooking U8 pin 1 to the trace just cut from U8 pin 2, which is A11.

6B. Wire U8 pin 2 to U1 pin 25 (A12). This can be done by hooking U8 pin 2 to the trace just cut from U8 pin 3, which is A12.

6C. Wire U8 pin 3 to U1 pin 26 (A13). This could also be wired to ground, but wiring it to A13 will allow more EPROMs to be added later on.

This completes the modification. Plug in a 2716 with some software in it and try it out.

Part 2, 2732 Wiring

5A. Wire the trace connecting U15 thru U18 together to U1 pin 24 (A11).

6A. Wire U8 pin 1 to U1 pin 25 (A12). A12 can be picked up from the trace just cut from U8 pin 3.

6B. Wire U8 pin 2 to U1 pin 26 (A13).

6C. Wire U8 pin 3 to U1 pin 27 (A14). Pin 3 could alternatively be hooked to ground if no additional EPROMs are going to be used.

This completes the 2732 modification. Plug in a 2732 with some good software in it and give it a try.

Additional Memory

These modifications leave room for further additions to both the EPROM and RAM space. To add more EPROMs might require some swift work, as additional EPROMs cannot be piggy-backed. One approach might be to kludge sockets onto the back of the board, and wire them to the present sockets, except for the chip-select pins. They are hooked to the remaining enable outputs from U8 (pins 11, 10, 9, 7) as required.

The RAM is easier to expand. Just piggy-back the additional 2114 chips on top of the present ones (U19 to U26) except for the chip selects (pin 8), which go to U27 pins 11, 10, 9, and 7. This will double the RAM on the board from 4k to 8k.

Make sure you remind whoever burns your EPROMs which ones you are using and that your RAM is now at 8000-8FFF hex. Happy packeting!!!

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